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Process For Making Bit Selectable Devices Having Elements Made With Nanotubes

Cross-Reference to Related Applications

[0001] This application claims priority under 35 USC §119(e) to the following application, which is hereby incorporated by reference in its entirety:

"Process For Making Bit Selectable Devices Having Elements Made With Nanotubes," U.S. Provisional Pat. Apl. Ser. No. 60/464472, filed on April 22, 2003.

[0002] The following applications are related and are hereby incorporated by reference in their entirety:

"Electro-Mechanical Switches and Memory Cells Using Horizontally-Disposed Nanofabric Articles and Methods of Making the Same", U.S. Provisional Pat. Apl. Ser. No. 60/446783, filed on February 12, 2003;

"Electro-Mechanical Switches and Memory Cells Using Vertically-Disposed Nanofabric Articles and Methods of Making the Same", U.S. Provisional Pat. Apl. Ser. No. 60/446786, filed on February 12, 2003;

"Combined Three Terminal and Four Terminal Nanotube /FET Structures", U.S. Provisional Pat. Apl. Ser. No. 60/512602, filed on October 16, 2003;

NRAM Bit Selectable Two-Device Nanotube Array", U.S. Apl. Ser. No. 10/810962, filed on March 26, 2004;

"NRAM Byte/Block Released Bit Selectable One-Device Nanotube Array", U.S. Apl. Ser. No. 10/810963, filed on March 26, 2004;

"Single Transistor With Integrated Nanotube (NT-FET)", U.S. Apl. Ser. No. 10/811191, filed on March 26, 2004; and

"Nanotube-On-Gate FET Structures And Applications", U.S. Apl. Ser. No. 10/811356, filed on March 26, 2004.

Background

1. Technical Field

[0003] The present application relates to the manufacture of devices using transistors and nanotube switching elements and in which the nanotube switching element records the informational state of the device.

2. Discussion of Related Art

[0004] Currently, most memory storage devices utilize a wide variety of energy dissipating devices which employ the confinement of electric or magnetic fields within capacitors or inductors respectively. Examples of state of the art circuitry used in memory storage include FPGA, ASIC, CMOS, ROM, PROM, EPROM, EEPROM, DRAM, MRAM and FRAM, as well as dissipationless trapped magnetic flux in a superconductor and actual mechanical switches, such as relays.

[0005] An FPGA (Field Programmable Gate Array) is a programmable logic device (PLD), a programmable logic array (PLA), or a programmable array logic (PAL) with a high density of gates, containing up to hundreds of thousands of gates with a wide variety of possible architectures. The ability to modulate (i.e. effectively to open and close) electrical circuit connections on an IC (i.e. to program and reprogram) is at the heart of the FPGA (Field programmable gate array) concept.

[0006] An ASIC (Application Specific Integrated Circuit) chip is custom designed for a specific application rather than a general-purpose chip such as a microprocessor. The use of ASICs can improve performance over general-purpose CPUs, because ASICs are "hardwired" to do a specific job and are not required to fetch and interpret stored instructions.

[0007] Important characteristics for a memory cell in electronic device are low cost, nonvolatility, high density, low power, and high speed. Conventional memory solutions include Read Only Memory (ROM), Programmable Read only Memory (PROM), Electrically Programmable Memory (EPROM), Electrically Erasable Programmable Read Only Memory (EEPROM), Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM).

[0008] ROM is relatively low cost but cannot be rewritten. PROM can be electrically programmed but with only a single write cycle. EPROM (Electrically-erasable programmable read-only memories) has read cycles that are fast relative to ROM and PROM read cycles, but has relatively long erase times and reliability only over a few iterative read/write cycles. EEPROM (or "Flash") is inexpensive, and has low power consumption but has long write cycles (ms) and low relative speed in comparison to DRAM or SRAM. Flash also has a finite number of read/write cycles leading to low long-term reliability. ROM, PROM, EPROM and EEPROM are all non-volatile, meaning that if power to the memory is interrupted the memory will retain the information stored in the memory cells.

[0009] EEPROMS are widely used within the computer industry to store a BIOS (basic input-output system) for a computer, sensor, or processing device, allowing it to load data and system instructions from other storage media when the unit receives first power after being in a quiescent state. The size of the BIOS is typically minimized in design because of the high cost of flash memory.

[0010] DRAM (dynamic random access memory) stores charge on capacitors but must be electrically refreshed every few milliseconds complicating system design by requiring separate circuitry to "refresh" the memory contents before the capacitors discharge. SRAM does not need to be refreshed and is fast relative to DRAM, but has lower density and is more expensive relative to DRAM. Both SRAM and DRAM are volatile, meaning that if power to the memory is interrupted the memory will lose the information stored in the memory cells.

[0011] Consequently, existing technologies are either non-volatile but are not randomly accessible and have low density, high cost, and limited ability to allow multiple writes with high reliability of the circuit's function, or they are volatile and complicate system design or have low density. Some emerging technologies have attempted to address these shortcomings.

[0012] For example, magnetic RAM (MRAM) or ferromagnetic RAM (FRAM) utilizes the orientation of magnetization or a ferromagnetic region to generate a nonvolatile memory cell. MRAM utilizes a magnetoresistive memory element involving the anisotropic magnetoresistance or giant magnetoresistance of ferromagnetic materials

yielding nonvolatility. Both of these types of memory cells have relatively high resistance and low-density. A different memory cell based upon magnetic tunnel junctions has also been examined but has not led to large-scale commercialized MRAM devices. FRAM uses a circuit architecture similar to DRAM but which uses a thin film ferroelectric capacitor. This capacitor is purported to retain its electrical polarization after an externally applied electric field is removed yielding a nonvolatile memory. FRAM suffers from a large memory cell size, and it is difficult to manufacture as a large-scale integrated component. See U.S. Patent Nos. 4,853,893; 4,888,630; 5,198,994, 6,048,740; and 6,044,008.

[0013] Another technology having non-volatile memory is phase change memory. This technology stores information via a structural phase change in thin-film alloys incorporating elements such as selenium or tellurium. These alloys are purported to remain stable in both crystalline and amorphous states allowing the formation of a bi-stable switch. While the nonvolatility condition is met, this technology appears to suffer from slow operations, difficulty of manufacture and poor reliability and has not reached a state of commercialization. See U.S. Patent Nos. 3,448,302; 4,845,533; and 4,876,667.

[0014] Wire crossbar memory (MWCM) has also been proposed. See U.S. Patent Nos. 6,128,214; 6,159,620; and 6,198,655. These memory proposals envision molecules as bi-stable switches. Two wires (either a metal or semiconducting type) have a layer of molecules or molecule compounds sandwiched in between. Chemical assembly and electrochemical oxidation or reduction are used to generate an "on" or "off" state. This form of memory requires highly specialized wire junctions and may not retain non-volatility owing to the inherent instability found in redox processes.

[0015] Recently, memory devices have been proposed which use nanoscopic wires, such as single-walled carbon nanotubes, to form crossbar junctions to serve as memory cells. See WO 01/03208, Nanoscopic Wire-Based Devices, Arrays, and Methods of Their Manufacture; and Thomas Rueckes et al., "Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing," Science, vol. 289, pp. 94-97, 7 July, 2000. Electrical signals are written to one or both wires to cause them to physically attract or repel relative to one another. Each physical state (i.e., attracted or repelled wires) corresponds to an electrical state. Repelled wires are an open circuit junction. Attracted

wires are a closed state forming a rectified junction. When electrical power is removed from the junction, the wires retain their physical (and thus electrical) state thereby forming a non-volatile memory cell.

[0016] The use of an electromechanical bi-stable device for digital information storage has also been suggested (c.f. US4979149: Non-volatile memory device including a micro-mechanical storage element).

[0017] The creation and operation of a bi-stable nano-electro-mechanical switches based on carbon nanotubes (including mono-layers constructed thereof) and metal electrodes has been detailed in a previous patents and patent application of Nantero, Inc. (U.S.S.N. 09/915093, 09/915173, 09/915095, 10/033323, 10/033032, 10/128118, 10/128117, 10/341005, 10/341055, 10/341054, 10/341130, 60/446783 and 60/446786, add 41 the contents of which are hereby incorporated by reference in their entireties).

[0018] Memory devices have been proposed which use nanoscopic wires, such as single-walled carbon nanotubes, to form crossbar junctions to serve as memory cells. (See WO 01/03208, Nanoscopic Wire-Based Devices, Arrays, and Methods of Their Manufacture; and Thomas Rueckes et al., "Carbon Nanotube-Based Nonvolatile Random Access Memory for Molecular Computing," Science, vol. 289, pp. 94-97, 7 July, 2000.) Hereinafter these devices are called nanotube wire crossbar memories (NTWCMs). Under these proposals, individual single-walled nanotube wires suspended over other wires define memory cells. Electrical signals are written to one or both wires to cause them to physically attract or repel relative to one another. Each physical state (i.e., attracted or repelled wires) corresponds to an electrical state. Repelled wires are an open circuit junction. Attracted wires are a closed state forming a rectified junction. When electrical power is removed from the junction, the wires retain their physical (and thus electrical) state thereby forming a non-volatile memory cell.

[0019] The NTWCM proposals rely on directed growth or chemical self-assembly techniques to grow the individual nanotubes needed for the memory cells. These techniques are now believed to be difficult to employ at commercial scales using modern technology. Moreover, they may contain inherent limitations such as the length of the nanotubes that may be grown reliably using these techniques, and it may difficult to

control the statistical variance of geometries of nanotube wires so grown. Improved memory cell designs are thus desired.

[0020] U.S. Patent Publication No. 2003-0021966 discloses, among other things, electromechanical circuits, such as memory cells, in which circuits include a structure having electrically conductive traces and supports extending from a surface of a substrate. Nanotube ribbons are suspended by the supports that cross the electrically conductive traces. Each ribbon comprises one or more nanotubes. The ribbons are formed from selectively removing material from a layer or matted fabric of nanotubes.

[0021] For example, as disclosed in U.S. Patent Application Publication No. 2003-0021966, a nanofabric may be patterned into ribbons, and the ribbons can be used as a component to create non-volatile electromechanical memory cells. The ribbon is electromechanically-deflectable in response to electrical stimulus of control traces and/or the ribbon. The deflected, physical state of the ribbon may be made to represent a corresponding information state. The deflected, physical state has non-volatile properties, meaning the ribbon retains its physical (and therefore informational) state even if power to the memory cell is removed. As explained in U.S. Patent Application Publication No. 2003-0124325, three-trace architectures may be used for electromechanical memory cells, in which the two of the traces are electrodes to control the deflection of the ribbon.

[0022] A typical nanotube device is composed of a nanofabric as described in U.S. patent application serial no. 09/915093, Electromechanical Memory Array Using Nanotube Ribbons and Method for Making Same, filed July 25, 2001 (NAN-1); U.S. patent application serial no. 09/915173, Electromechanical Memory Having Cell Selection Circuitry Constructed with Nanotube Technology, filed July 25, 2001 (NAN-2);

[0023] U.S. patent application serial no. 09/915095, Hybrid Circuit Having Nanotube Electromechanical Memory, July 25, 2001 (NAN-3); U.S. patent application serial no. 10/033323, Electromechanical Three-Trace Junction Devices, filed December 28, 2001 (NAN-4); U.S. patent application serial no. 10/033032, Methods Of Making Electromechanical Three-Trace Junction Devices, filed December 28, 2001 (NAN-5); U.S. patent application serial no. 10/128118, Nanotube Films And Articles, filed April

23, 2002, (NAN-6); U.S. patent application serial no. 10/128117, Methods Of Nanotube Films And Articles, filed April 23, 2002 (NAN-7); U.S. patent application serial no. 10/341005, Methods Of Making Carbon Nanotube Films, Layers, Fabrics, Ribbons, Elements And Articles, filed January 13, 2003 (NAN-15); U.S. patent application serial no. 10/341055, Methods Of Using Thin Metal Layers To Make Carbon Nanotube Films, Layers, Fabrics, Ribbons, Elements And Articles, filed January 13, 2003 (NAN-16); U.S. patent application serial no. 10/341054, Methods Of Using Pre-Formed Nanotubes To Make Carbon Nanotube Films, Layers, Fabrics, Ribbons, Elements And Articles, filed January 13, 2003 (NAN-17); and U.S. patent application serial no. 10/341130, Carbon Nanotube Films, Layers, Fabrics, Ribbons, Elements And Articles, filed January 13, 2003 (NAN-18). In at least some cases, to create a nanofabric, the technique chosen must result in a sufficient quantity of nanotubes in contact with other nanotubes which thereby matte as a result of the nanotubes' adhesion characteristics. Certain embodiments (e.g., memory cells) benefit when the nanofabric is very thin (e.g., less than 2nm); for example, when the nanofabric is primarily a monolayer of nanotubes with sporadic overlapping (sometimes fabric will have portions that are bilayers or trilayers), or a multilayer fabric with relatively small diameter nanotubes. Moreover, many of these embodiments benefit when the nanotubes are single-walled nanotubes (SWNTs). Other embodiments (e.g., conductive traces) may benefit from thicker fabrics or multi-walled nanotubes (MWNTs). The nanofabric is patterned using photolithographic techniques generating an electrically conductive trace of nanotubes, NT.

Summary

[0024] The present invention provides a process for making bit selectable devices having elements made with nanotubes.

[0025] Under one aspect of the invention, a method is used to make a bit selectable device having nanotube memory elements. A structure having at least two transistors is provided, each with a drain and a source with a defined channel region therebetween, each transistor further including a gate over said channel. A trench is formed between one of the source and drain of a first transistor and one of the source and drain of a second transistor. An electrical communication path is formed in the trench between one

of the source and drain of a first transistor and one of the source and drain of a second transistor. A defined pattern of nanotube fabric is provided over at least a horizontal portion of the structure and extending into the trench. An electrode is provided in the trench. A pattern of nanotube fabric is suspended so that at least a portion is vertically suspended in spaced relation to the vertical walls of the trench and positioned so that the vertically suspended defined pattern of nanotube fabric is electromechanically deflectable into electrical communication with one of the drain and source of a first transistor and one of the source and drain of a second transistor.

[0026] Under another aspect of the invention, a defined pattern of nanotube fabric includes the application of pre-formed nanotubes to create a layer of nanotubes.

[0027] Under another aspect of the invention, the layer is substantially a monolayer of nanotubes.

[0028] Under another aspect of the invention, the layer is a highly porous fabric of nanotubes.

[0029] Under another aspect of the invention, the layer of nanotubes is a conformal fabric of nanotubes.

[0030] Under another aspect of the invention, the nanotubes are single walled carbon nanotubes.

[0031] Under another aspect of the invention, the suspended length of nanotube fabric has an extent that is sub-lithographic-critical-dimension.

Brief Description of the Drawings

[0032] In the Drawings,

Figures 1-24 are figures illustrating sequential steps involved in the methods according to certain embodiments of the invention;

Figure 25 is a cell layout according to one embodiment of the invention.

Detailed Description

[0033] The device made by the present invention can be described by its cell size. For a bit selectable, bit erasable cell, a 2T-cell (two transistor) the minimum cell size would be 12 F^2, (F^2 is a reference to the smallest feature size, squared.) Advantages of using this method include, that most likely no new tooling would be required to perform

the methods in a fabrication plant. Nanotubes are dispensed by regular spin-coating and patterned using traditional lithography. Nanotube switching element requires controlled air gap and anchor to structures adjacent to the gap.

[0034] Figure 1 illustrates a first intermediate structure 100 from a method of fabricating the article according to one aspect of the invention.

[0035] A silicon wafer substrate 110, having diffusion regions 120, gates 130 and nitride 140, covering the gates, is provided or created; alternatively, the substrate may be made from any material suitable for use with lithographic etching and electronics. The appropriate ground rule for the following processes is dependent upon the desired device performance and application, but the process flow is compatible with lithographic processes from many microns to sub 100 nm and below. Embedded in substrate 110 are diffusion regions 120. Gate material can be any material suitable for creation of a field effect on the adjacent substrate and source and drain regions, including but not limited to; metals, conductors or semiconductors, including nanofabric made of carbon nanotubes. Gates 130 are covered by first nitride layer 140 or other suitable dielectric, first nitride layer 140 having substantially planar top surface 150.

[0036] Figure 2 illustrates intermediate structure 200 in cross sectional view and plan view. Oxide layer 210 is deposited on intermediate structure 100 and is planarized such that the top surface of oxide layer 210 is substantially level with nitride top surface 150, as illustrated: gate direction line 230 is shown as dotted lines.

[0037] Etch line 310 extending between and adjacent to gates 130 are etched and polysilicon is deposited in the spaces created by etching such that the polysilicon fills the spaces adjacent to gates 130; polysilicon regions 320 are thus created. Etch lines 310 are preferably oriented orthogonally to gate line 230. Alternatively polysilicon regions can be made from other metallic, conducting or semiconducting materials consistent with the desired use of the article. Top surfaces of polysilicon regions 320 are made substantially level with top surface 150, e.g. by CMP (chemical-mechanical polishing), forming intermediate structure 300 as illustrated by Figure 3. It is not necessary that polysilicon be used for such regions and other materials may be used.

[0038] Second nitride layer 410 is applied to intermediate structure 300, forming intermediate structure 400. Exposed nitride 420, shown within dotted lines in Figure 4, is

removed, e.g. by lithographic patterning and etching, forming intermediate structure 500, shown in Figure 5, (Lithography mask not shown). It is not necessary that this or subsequent “nitride layers” be made of nitride, a suitable material will also serve the desired purpose of protecting nanotubes from subsequent depositions and to create spacers of proper dimensions with selectivity in etching over other elements, e.g. oxide layer 210 and polysilicon region 320.

[0039] Exposed polysilicon layer 510 (shown within dotted lines) and a region of underlying silicon 520 are removed, e.g. by etching, forming trench 610, and thereby forming intermediate structure 600, as shown in Figure 6. Alternatively, trench depth can be as deep as approximately the middle of polysilicon region 320, i.e. point 620, the trench may end at substrate interface point 630 or somewhere within the substrate, as shown in figure 6. Trench depth will depend on feature size, height 640 and materials used.

[0040] Third nitride layer 710 is deposited over top surfaces of intermediate structure 600, forming intermediate structure 700. Intermediate structure 700 having trench 720, as shown in Figure 7

[0041] Metal layer 810 is deposited in trench 720 forming intermediate structure 800 as shown in Figure 8. The deposition can be done in any appropriate manner including by sputtering, chemical vapor deposition (CVD) or by evaporation, followed by etch back if necessary, resulting in intermediate structure 800. Metal 810 may be any suitable conductor or semiconductor depending on the ultimate use of the article.

[0042] Figures 9-11 illustrate patterning of nanofabrics. Nanofabric 910 is applied to intermediate structure 800, thereby creating intermediate structure 900 as shown in Figure 9. Nanofabrics are preferably created by spin coating a suspension of nanotubes onto a planar or non-planar surface as described in incorporated references 10/128,118 and 10/341,005; however nanofabrics may be applied by any appropriate means.

[0043] Nanofabric patterning mask 1010 is applied over desired nanofabric sections 1020, as described in 09/915,095 and 10/341,005. Exposed nanofabric 1030 is removed, e.g. by ashing, leaving desired nanofabric sections 1020. Mask 1010 is stripped, using an appropriate stripper, such that desired nanofabric sections 1020 and intermediate structure 1000 are left substantially intact, leaving intermediate structure 1100, as shown

in Figure 11. Figure 11 illustrates cross sectional and plan views of intermediate structure 1100, and especially illustrates the three-dimensionality of nanofabric 910 and that it conforms to a non-planar surface.

[0044] Fourth nitride layer 1210, having top surface 1215, is applied to intermediate structure 1100, creating intermediate structure 1200; intermediate structure 1200 having trench 1220 (shown in plan view within dotted lines), as illustrated in Figure 12. Figure 12 illustrates cross sectional and plan views of intermediate structure 1200.

[0045] Oxide 1310 is deposited by any appropriate method, e.g. by use of an HDP tool or other appropriate mechanism, into trench 1220. If necessary, excess oxide is removed from top surface 1215 by any appropriate means, e.g. by CMP, such that the exposed top of oxide layer 1310 is substantially level with top surface 1215, thus forming intermediate structure 1300, as illustrated in Figure 13.

[0046] Figure 14 illustrates a plan view and a cross sectional view (taken at line 1410, shown as a dotted line) of intermediate structure 1400. Oxide 1310 is removed, e.g. by etching from active regions 1420 as illustrated in intermediate structure 1400, e.g. by using a line mask (not shown), line mask would preferably be substantially parallel to etch line 310.

[0047] Figure 15 illustrates a plan and a cross sectional view (taken at line 1410, shown as a dotted line) of intermediate structure 1500. Oxide 1510 is deposited on intermediate structure 1400, e.g. by use of a high density plasma (HDP) tool, forming intermediate structure 1500: oxide 1510 having oxide sidewall 1520.

[0048] Figure 16 illustrates a plan and a cross sectional view (taken at line 1410, shown as a dotted line) of intermediate structure 1600. Mask 1610 is applied to intermediate structure 1500, covering approximately one half of active regions 1420, leaving oxide sidewall 1520 exposed, as shown in Figure 16.

[0049] Figure 17 illustrates a plan view and a cross sectional view (taken at line 1410, shown as a dotted line) of intermediate structure 1700. Oxide sidewall 1520 is removed, e.g. by etching, thereby removing oxide sidewall 1620 and exposing nitride sidewall 1710. Mask 1610 is stripped by any appropriate method, thereby creating intermediate structure 1700.

[0050] Nitride sidewall 1710 is removed, e.g. by etching to expose contact to source/drain region 1810, thereby creating intermediate structure 1800, as illustrated in Figure 18. Contact to source/drain region 1810 is analogous to RN in figure 25 and is preferably located on release layer side of the structure.

[0051] Thin conductor layer 1910 is deposited over intermediate structure 1800, thereby creating intermediate structure 1900 as illustrated in Figure 19: thin conductive layer 1910 having vertical conductive portions 1920. Thin conductive layer 1910 can be made from any conductive material including but not limited to doped polysilicon.

[0052] Fifth nitride layer 2010 is deposited over intermediate structure 1900, thereby creating intermediate structure 2000 as illustrated in Figure 20: fifth nitride layer 2010 having horizontal nitride portions 2020 and vertical nitride portions 2030.

[0053] Horizontal nitride portions 2020 are removed, e.g. by directional etching or by reactive ion etching, thereby exposing horizontal conductive portions 2110 and creating intermediate structure 2100, as illustrated by Figure 21.

[0054] Horizontal conductive portions 2110 are removed, e.g. by etching, thereby creating channels 2210, and exposing exposed oxide portion 2220, thus creating intermediate structure 2200, as illustrated in Figure 22.

[0055] Exposed oxide portion 2220 is removed, e.g. by etching, thereby exposing exposed nitride portions 2310, leaving intermediate structure 2300, as illustrated in Figure 23.

[0056] Exposed nitride portions 2310 and vertical nitride portions 2030 are removed, by, e.g. etching, leaving suspended nanofabric portion 2410. Conductive plug 2420 is disposed between vertical conductive portions 1920, thus creating structure 2400 as illustrated by Figure 24. Conductive plug 2040 is disposed by any appropriate method including, but not limited to deposition and subsequent planarization. Conductive plug 2420 can be made from any appropriate conducting or semiconducting material consistent with the final use of the article. Care should be taken to ensure that the spaces around suspended nanofabric portion 2410 are left substantially free of conductive plug material.

[0057] Figure 25 illustrates a <u>Bit-Erasable 12 F^2 cell layout</u> wherein switching node(SN), release node(RN) and reference node(REF) form 3 terminals of device.

Voltage between SN and REF results in "ON" state (nanotubes flex to contact SN). Voltage between REF and RN results in "OFF" state irrespective of previous state. The voltages on SN and RN are controlled by potential to gates of switching and release transistors, TS and TR, respectively.

Alternate Embodiments

[0058] In some embodiments, having a nanofabric ribbon or other nanofabric article disposed adjacent to the movable nanofabric element instead of a metallic electrode permits removal of sacrificial materials from below the top electrode. Note that the electrodes may themselves be formed of nanofabric materials. Fluid may flow through a nanofabric material disposed above a sacrificial layer to remove the sacrificial material. Likewise, the lower electrode may be formed of a nanofabric material if desired.

[0059] Under certain preferred embodiments, a nanotube patch has a width of about 180 nm and is strapped, clamped, or pinned to a support preferably fabricated of silicon nitride. The local area of a contact electrode e.g. 620 forms an n-doped silicon electrode and is positioned close to the supports 110 and preferably is no wider than the deflecting nanotube patch, e.g., 180 nm. The relative separation between undeflected nanotube fabric and the contact electrode, (i.e. to the deflected position where the patch attaches to electrode) should be approximately 5-50 nm. The magnitude of the separation is designed to be compatible with electromechanical switching capabilities of the memory device. For this embodiment, the 5-50 nm separation is preferred for certain embodiments utilizing patch made from carbon nanotubes, but other separations may be preferable for other materials. This magnitude arises from the interplay between strain energy and adhesion energy of the deflected nanotubes. These feature sizes are suggested in view of modern manufacturing techniques. Other embodiments may be made with much smaller (or larger) sizes to reflect the manufacturing equipment's capabilities.

[0060] The nanotube patch of certain embodiments is formed from a non-woven fabric of entangled or matted nanotubes (more below). The switching parameters of the ribbon resemble those of individual nanotubes. Thus, the predicted switching times and voltages of the ribbon should approximate the same times and voltages of nanotubes. Unlike the prior art which relies on directed growth or chemical self-assembly of

individual nanotubes, preferred embodiments of the present invention utilize fabrication techniques involving thin films and lithography. This method of fabrication lends itself to generation over large surfaces especially wafers of at least six inches. The ribbons should exhibit improved fault tolerances over individual nanotubes, by providing redundancy of conduction pathways contained with the ribbons. (If an individual nanotube breaks other tubes within the rib provide conductive paths, whereas if a sole nanotube were used the cell would be faulty.)

[0061] While the inventors typically desire a monolayer fabric of single-walled nanotubes, for certain applications it may be desirable to have multilayer fabrics to increase current density, redundancy or other mechanical or electrical characteristics. Additionally it may be desirable to use either a monolayer fabric or a multilayer fabric comprising MWNTs for certain applications or a mixture of single-walled and multi-walled nanotubes. The previous methods illustrate that control over catalyst type, catalyst distribution, surface derivitization, temperature, feedstock gas types, feedstock gas pressures and volumes, reaction time and other conditions allow growth of fabrics of single-walled, multi-walled or mixed single- and multi-walled nanotube fabrics that are at the least monolayers in nature but could be thicker as desired with measurable electrical characteristics.

[0062] The effect of the van der Waals interaction between nanofabrics and other elements can be affected at their interface(s). The effect may be enhanced or diminished; for example, the attractive force can be diminished by coating the surface of the electrode with a thin layer of oxide or other suitable chemicals. Volatile nanoswitches may also be made by employing such techniques instead of or in addition to controlling the gap dimension between a patch and electrode. Such volatile switches may be especially useful in applications such as relays, sensors, transistors, etc.

[0063] As the vertical separation between the patch and the underlying electrode increases, the switch becomes volatile when the deflected nanofabric has a strain energy greater than that of the van der Waals force keeping the fabric in contact with the underlying electrode. The thicknesses of insulating layers which control this separation can be adjusted to generate either a non-volatile or volatile condition for a given vertical gap as called for by particular applications with desired electrical characteristics.

[0064] Other embodiments involve controlled composition of carbon nanotube fabrics. Specifically, methods may be employed to control the relative amount of metallic and semiconducting nanotubes in the nanofabric. In this fashion, the nanofabric may be made to have a higher or lower percentage of metallic nanotubes relative to semiconducting nanotubes. Correspondingly, other properties of the nanofabric (e.g., resistance) will change. The control may be accomplished by direct growth, removal of undesired species, or application of purified nanotubes. Numerous ways have been described, e.g. in the incorporated references, supra, for growing and manufacturing nanofabric articles and materials.

[0065] The U.S. Patent Applications, identified and incorporated above, describe several (but not limiting) uses of nanofabrics and articles made therefrom. They also describe various ways of making such nanofabrics and devices. For the sake of brevity, various aspects disclosed in these incorporated references are not repeated here. For example, the various masking and patterning techniques for selectively removing portions of the fabric are described in these applications; in addition, various ways of growing nanofabrics or of forming nanofabrics with preformed nanotubes are described in these applications.

[0066] As explained in the incorporated references, a nanofabric may be formed or grown over defined regions of sacrificial material and over defined support regions. The sacrificial material may be subsequently removed, yielding suspended articles of nanofabric. See, for example, Electromechanical Memory Array Using Nanotube Ribbons and Method for Making Same (U.S. Pat. Apl. Ser. No. 09/915,093) filed July 25, 2001, for an architecture which suspends ribbons of nanofabric Electro-Mechanical Switches, Memory Cells Using Horizontally-Disposed Nanofabric Articles and Methods of Making the Same (U.S. Pat. Apl. Ser. No. 60/446783) filed February 12, 2003 and Memory Cells Using Vertically-Disposed Nanofabric Articles and Methods of Making the Same (U.S. Pat. Apl. Ser. No. 60/446786) filed February 12, 2003.

[0067] Under certain embodiments, the technique of vertically suspending the nanotube fabric allows the suspended extent to be a function of thin film techniques. As a result, the suspended extent may be shorter than the minimum distances available with

the photolithography tools being employed; that is, the suspended extent may be sub-critical-dimension.

[0068] Under certain embodiments, the fabric may be highly porous fabric of single-walled carbon nanotubes. Moreover, the fabric may be substantially a monolayer of nanotubes.

[0069] The articles formed by preferred embodiments help enable the generation of nanoelectronic devices and may also be used to assist in increasing the efficiency and performance of current electronic devices using a hybrid approach (e.g., using nanoribbon memory cells in conjunction with semiconductor addressing and processing circuitry).

[0070] A nanofabric or ribbon has been shown to substantially conform to a surface, such as a surface of an article on a semiconductor substrate. A fabric of nanotubes may be constructed by any appropriate means, including, but not limited to spin coating, direct growth on a suitable substrate or other application. The fabric will be horizontally oriented when the surface of the substrate that receives the fabric is horizontally oriented. The present inventors have appreciated that devices such as electro-mechanical switches can be constructed using nanofabrics which have conformed to a surface which is substantially perpendicular to a semiconductor substrate (vertically-oriented) and that such devices can be used as vertically oriented switches in a plethora of applications. Fabrication techniques to develop such horizontally- and vertically-disposed fabrics and devices composed of nanotube fabrics which comprise redundant conducting nanotubes may be created via CVD, or by room temperature operations as described herein and described in applications U.S.S.N. 09/915093, 09/915173, 09/915095, 10/033323, 10/033032, 10/128118, 10/128117, 10/341005, 10/341055, 10/341054, 10/341130, 60/446783 and 60/446786, the contents of which are hereby incorporated by reference in their entireties. Such fabrication techniques include the ability to form said switches for use in many different articles having relatively short spans of suspended nanofabric articles. In some embodiments, this allows smaller device dimensions and higher strains in the nanofabric articles, as well as lower electrical resistances. Such articles may be adapted or modified to perform logic functions or be part of a scheme involving logical functionality.

[0071] Volatile and non-volatile switches, and switching elements of numerous types of devices, can be thus created. In certain preferred embodiments, the articles include substantially a monolayer of carbon nanotubes. In certain embodiments the nanotubes are preferred to be single-walled carbon nanotubes. Such nanotubes can be tuned to have a resistance between 0.2- 100 kOhm/□ or in some cases from 100 kOh/□ to 1GOhm/□.

[0072] The logic circuitry of the present invention generally operate using non-volatile operation/switching of nanotubes, although non-volatile operation of nanofabric switches is within the scope of the present invention. In addition, coordination of volatile and non-volatile elements may be advantageous for generating simultaneously logic and memory functions or as part of an overall logic functionality. It is CMOS built with only nanoelectromechanical nanofabric structures constructed with carbon nanotubes. It does not necessarily draw DC current and may only dissipate power when it switches.

[0073] It will be further appreciated that the scope of the present invention is not limited to the above-described embodiments but rather is defined by the appended claims, and that these claims will encompass modifications and improvements to what has been described.

[0074] What is claimed is: